REMARKS

Favorable reconsideration of this application is respectfully requested.

The present invention relates to storage switch architectures and methods for use in storage area networks (SANs) that afford high bandwidth and substantially improved performance and simplicity over conventional storage switches and switching systems. Storage switch architectures and methods in accordance with the invention enable multi-protocol SANs that are capable of processing data packets for virtualization at "wire speed", i.e., at the incoming speed of the packet at a switch port without introducing any more latency than would be introduced by a switch that merely performed switching or routing functions. This affords switches which are able to process data without buffering data packets as is done in conventional switches. Thus, compared with conventional practices, switch architectures and methods in accordance with the invention minimize the time required to process packets, and have a higher throughput rate than conventional switches.

The various rejections of Claims 1-35 under 35 U.S.C. §103 as being obvious over the published U.S. patent applications US 2002/0116535 to Ryals et al. and US 2003/0236945 to Nahum, together or in combination with U.S. Pat. No. 6,775,706 to Fukumoto et al. are respectfully traversed. For the reasons discussed below, it is respectfully submitted that the cited prior art neither discloses nor suggests the invention claimed, and that the claims are patentable over this prior art.

This application contains twelve independent claims. These are independent method Claims 1, 9, 10, 12, 14 and 19, independent switch Claims 24, 29 and 32, independent linecard Claims 30 and 31, and an independent Claim 34 directed to a computer program. With the exception of independent Claims 14 and 19, all of the independent claims in this application (as well as a number of the dependent claims) recite either one of two different elements which are not taught or suggested by the cited prior art. Accordingly, these elements distinguish over the cited prior art, and render the claims patentable.

As will be explained more fully below, these two different distinguishing claim elements are: (i) that the claimed method or switch operates on packets "without buffering the packet", and (ii) that the method or switch operates "at wire speed". Therefore, the independent claims that recite either of these two elements (and the claims which depend therefrom) are allowable over the prior art for at least this reason. Independent Claims 14 and 19 distinguish over the prior art and are allowable for other reasons, as discussed below.

The significant advantages afforded by the invention are due, in part, to the fact that switches in accordance with the invention distribute intelligence to every switch port, which enables data packets to be processed at wire speed and without buffering, i.e., without introducing any more latency than would be introduced by a switch that merely performed switching or routing functions (see specification, page 13, paragraph [0062], lines 1-4). In particular, as used in the specification (see page 13, paragraph [0062]), the term "wire speed" is defined to be a speed measured by the connection to

a particular switch port. Thus, "wire speed" means that a storage switch can handle the maximum packet throughput rate for the type of connection to a switch port. For example, as described on page 13, if the connection to a port is an OC-48 connection (2.5 bits per nsec), wire speed means that the switch must keep up with that data rate. Similarly, if a switch port is 1 Gb Ethernet, wire speed processing will be 1 bit per nsec; and if it is the port is 2 Gb Fibre Channel, the wire speed will be 5 µsec per Kilobyte, etc. Typically, in order to process data at wire speed, a storage switch in accordance with the invention will not buffer packets, as is done in conventional switches (see specification, page 6, paragraph [0015]). Rather, switches in accordance with the invention have an architecture that minimizes the processing time for packets to enable wire speed to be met.

I. Without Buffering

Independent Claims 1, 10, 12, 24, 30, 32 and 34, as well as dependent Claims 17 and 21 explicitly recite that processing of packets occurs "without buffering". None of the prior art references cited by the Office teach or suggest a method or switch, as claimed, where data packets are processed "without buffering".

The primary reference relied upon by the Office in rejecting all claims is Ryals, et al. ("Ryals"). Ryals discloses a data switching device that switches data between input ports and output ports on different interface cards of the switching device. As shown in Figure 4 of Ryals, data is switched between ports 436, 438 and 440 on one interface card 402 to ports 442, 444 and 446 on a second interface card 448. Each of the interface cards is connected to a backplane bus 428 over which data is transferred

between the cards, and each card is also connected to a separate control bus 430 which is used for controlling the ports to which data packets are routed.

As is plainly shown in Figure 4, and as described in the published Ryals application (see paragraphs [0036] and [0042]), interface card 402 has a main buffer 404 connected to ports 436, 438 and 440 for buffering data to and from those ports and the backplane 428, and interface card 448 has a main buffer 418 that performs a similar function for data flowing to and from ports 442, 444 and 446. Ryals expressly states that the buffers are employed for storing data cells arriving and leaving the switch via the ports. Thus, Ryals explicitly teaches away from independent Claims 1, 10, 12, 24, 30, 32 and 34, as well as dependent Claims 17 and 21 that require data processing without buffering, and cannot support a rejection of such claims.

The other reference relied upon by the Office in it's rejections is the published application to Nahum. This application, however, merely discloses associating a storage virtualization manager (SVM) with a network switch, and describes the operation of the SVM in switching data packets. It does not address or disclose at all the internal structure of the switch, and does not disclose or teach a switch that processes data packets "without buffering".

In the Office's rejection of Claims 1, 8, 9, 10, 12, 14, 15, 17, 18, 24, and 25-35, (see Office Action, page 2, paragraph 1, subparagraph 5) the Office notes that Ryals discloses “a buffer within an interface card . . . ”, referencing Figure 4, and states “as does the present application, which contains a buffer in combination with the TM within a line card”.

First, as the Office recognizes and admits, Ryals, in fact, discloses a buffer in an interface card. However, what the rejection overlooks is that it is the claims that set out the invention and which are supposed to be examined, not the specification. It is irrelevant what is disclosed in embodiments in applicants' specification, the claims require that data packets be processed "without buffering". Ryals discloses and teaches buffering, and thus teaches away from the claimed invention. Furthermore, none of the other two cited prior art references teach or suggest processing packets in a linecard "without buffering", as claimed. Therefore, the cited references do not teach or suggest to one skilled in the art the invention claimed, and cannot support a rejection based upon obviousness for this reason alone.

II. At Wire Speed

With respect to the other distinguishing element of the claims regarding processing packets at wire speed, independent Claim 9, 29, 31 and 32, as well as dependent Claims 2, 11, 13, 16, 20, 25, and 35, all explicitly recite, among other things, that packets are processed at wire speed. As discussed above, the specification defines wire speed relative to the speed of the connection to a particular port of the switch on which packets are sent or received. None of the cited prior references disclose or suggest this element of the claimed invention.

Contrary to the Office's assertion, (see, for example, the rejection of Claims 2, 11, 13 and 16, on page 3 of the Office Action, as well as the rejections of other claims, such as Claim 20 on page 7), Ryals does not disclose processing packets at wire speed, as claimed. As to paragraph [0028] of Ryals, referred to by the Office, that

paragraph merely discloses that interface cards are configured to support the maximum transfer rate of backplane of the switch. The "maximum transfer rate of the backplane" is not the same as wire speed, as claimed. Ryals, in fact, discloses nothing with respect to processing data packets at the speed with which they are received from or sent to ports of the switch, nor does Ryals disclose anything with respect to packet rates for port connections. The speed of the backplane bus of Ryals over which packets are transferred to and from the main buffers 404 and 418 of the interface cards 402 and 448 has nothing to do with the packet speed at the ports of each card since Ryals buffers packets.

Since Ryals does not teach or suggest processing packets at the "wire speed" of the switch ports, as claimed, Ryals cannot render obvious independent Claims 9, 29, 31 and 32, or dependent Claims 2, 11, 13, 16, 20, 25 and 35, which explicitly recite processing packets at "wire speed". Moreover, neither of the other prior art references cited teaches or suggests processing packets at wire speed. Accordingly, no combination of this cited prior art can render these claims obvious.

III. Independent Claims 14 and 19

As to independent Claims 14 and 19, and the dependent Claims 15-18 and 20-23 which depend from Claims 14 and 19, the cited prior art also fails to disclose or suggest the recitations of these claims. In particular, Claim 14 calls for a method for use in a switch in a storage network wherein an ingress linecard receives information about a virtual target, including a flowID, and places a virtual target descriptor identifier and the flowID in a local header of a packet, affords the packet to a fabric, which

affords the packet to an egress line card in accordance with the flowID, and where the egress line card converts a virtual target block address to a physical target block address, as claimed. Nothing in the prior art cited discloses or suggests a line card updating headers in data packets with virtual target descriptor identifiers or flowIDs, as claimed.

Dependent Claim 15, which depends from Claim 14, further calls for the ingress line card placing a trace tag in the local header where the trace tag identifies stored information about a request. As discussed above, there is no disclosure in the prior art of placing tags in local headers of data packets.

Claim 16, which depends from Claim 14, calls for the steps to be performed at wire speed, and is allowable for the reasons discussed above.

Claims 17, which depends from Claim 14, calls for the steps to be performed without buffering the packet, and is allowable for the reasons discussed above.

Independent Claim 19 is directed to a method for use as a switch storage network which calls for adding and then subsequently removing a local header to a packet, placing an ingress task control block index and virtual target descriptor identifier into the local header, retrieving flowID from the virtual target descriptor and placing the flowID into the local header, using the virtual target descriptor identifier, retrieving a physical target descriptor identifier, allocating an egress task control block with a control block index, and using information in the physical target descriptor to convert the virtual target address to a physical target address, as claimed. There is

nothing even remotely suggestive of the elements of Claim 19 in any of the references cited. Accordingly, the rejection of Claim 19 based upon the cited prior art is improper, and Claim 19 is deemed allowable.

Claim 20 recites that the steps of Claim 19 are performed at wire speed; and Claim 21 recites they are performed without buffering, and are allowable for reasons previously discussed.

The foregoing has pointed out only some of the elements that are not taught or suggested by the cited prior art, and discussed only some of the reasons that the claims are allowable. Generally, the Office's rejections of the claims focus on a few broad generalities, and do not consider many of the specific recitations of the claims. As such, the rejections fail to consider the invention as a whole, and are improper for this reason.

It is clear form the foregoing that there is no disclosure or suggestion in the prior art cited of either processing packets without buffering, or processing packets at wire speed, as claimed. Accordingly, the cited prior art cannot render Claims 1 – 13, 16 - 18, and 20 - 35 obvious, and the rejections of these claims should be withdrawn.

As to Claims 14, 15 and 19, for the reasons pointed out above, the prior art also fails to disclose or suggest the recitations of these claims.

In view of the foregoing, it is respectfully submitted that the cited prior art cannot render any of Claims 1-35 unpatentable under 35 U.S.C. §103, and that the rejections

of the claims on this basis should be withdrawn, and that this application is in condition for allowance. Early allowance of all claims is solicited.

The specification has been amended to update the status of the applications referred to on page 1 - 2.

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Respectfully Submitted,

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